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PATENT APPLICATION

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IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s):	Duane E. Galbi
Serial No.:	09/919,283
Examiner:	Robert C Scheibel
Filing Date:	07/31/2001
Group Art Unit:	2666
Title:	METHOD FOR AUTOMATIC RESOURCE RESERVATION AND COMMUNICATION THAT FACILITATES USING MULTIPLE PROCESSING EVENTS FOR A SINGLE PROCESSING TASK

MAILSTOP: APPEAL BRIEF-PATENTS
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BRIEF ON APPEAL

INTRODUCTION

Pursuant to the provisions of 37 CFR § 1.191 *et seq.*, applicants hereby appeal to the Board of Patent Appeals and Interferences (the "Board") from the examiner's final rejection dated 8/3/2005. A notice of appeal was sent on the same day as this appeal brief. This brief on appeal is accompanied by the requisite fee (37 CFR 41.20(b)(2)).

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REAL PARTY IN INTEREST

The entire interest in the present application has been assigned to Conexant Systems, Inc. as recorded at Reel 012525, Frame 0093.

RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

STATUS OF CLAIMS

Claims 1, 3, 5, 6, 10, 11, 13, 15, 16, and 20 are pending.

Claims 2, 4, 7 – 9, 12, 14, 17 – 19, and 21 have been canceled.

Claims 1, 3, 5, 6, 10, 11, 13, 15, 16, and 20 have been finally rejected.

Claims 1, 3, 5, 6, 10, 11, 13, 15, 16, and 20 are on appeal.

STATUS OF AMENDMENTS

The specification has a number of amendments pending that correct some informalities in the status of several applications listed in the current application.

Claim 1 has an amendment pending to correct a grammatical informality.

SUMMARY OF CLAIMED SUBJECT MATTER

The independent claims involved in the appeal are listed below with references inserted into the body of the claims indicating line and page numbers and drawing references.

1. An integrated circuit (100) for processing events related to communication packets, said integrated circuit comprising:

a core processor (104) configured to execute software to process a series of communication packets, the processing of each packet being an event and having associated data and context information (page 7 line 27 – page 8 line 3); and

a co-processor (107) comprising a plurality of state information buffers (314, 620) for storing state information, a plurality of context buffers (315) for storing context

information associated with a plurality of events and a plurality of data buffers (314, 614) for storing data associated with the plurality of events where the state information comprises a data buffer pointer pointing to one of the plurality of data buffers (614) and a context buffer pointer pointing to one of the plurality of context buffers (615)(page 14 lines 3 – 27, page 20 line 24 – page 22 line 6);

the state information is associated with events wherein each of said state information buffers (620) having an in-use counter (620-0) indicating the number of events associated with the contents of said buffer (page 22 line 28 – page 23 line 14).

10. An integrated circuit (100) for processing events related to communication packets, said integrated circuit comprising:

a core processor (104) configured to execute software to process a series of communication packets, the processing of each packet being an event and having associated data and context information (page 7 line 27 – page 8 line 3); and

a co-processor (107) comprising a plurality of state information buffers (314, 620) for storing state information associated with events wherein each of said state information buffers (314, 620) having an in-use counter (620-0) indicating the number of events associated with the contents of said buffer, wherein said co-processor (107) comprises a plurality of data only information buffers (614), a plurality of context information buffers (615), an in-use counter for each of said data only buffers and an in-use counter for each of said context buffers)(page 14 lines 3 – 27, page 20 line 24 – page 22 line 6) where data can be passed from one event to another event by changing the data in one of said state information buffers and where the state information comprises a data only buffer pointer pointing to one of the plurality of data only information buffers and a context information buffer pointer pointing to one of the pluralities of context information buffers (page 22 line 28 – page 23 line 14).

11. A method of processing events related to communication packets in an integrated circuit

which includes a core processor (104) and a co-processor (107) having a state information buffer (620) for storing state information, a context buffer (615) for storing context information and a data buffer (614) for storing data where the state information comprises a data buffer pointer and a context pointer-where the data buffer pointer points to the data buffer and the context pointer points to the context buffer (page 14 lines 3 – 27, page 20 line 24 – page 22 line 6), the state information for an event is stored separate from the data associated with said event, said state information buffer having an associated in use counter, the method comprising:

incrementing the in-use counter associated with said state information buffer when an event is associated with said state information buffer; and

decrementing the in-use counter of said state information buffer when said event associated with said buffer is finished (page 22 line 28 – page 23 line 14).

16. An integrated circuit (100) for processing events associated with communication packets which includes a core processor (104) and a co-processor (107), the improvement which comprises, separate buffers for data (614), context (615), and state information (620) and in-use counters for all of said buffers (page 14 lines 3 – 27, page 20 line 24 – page 22 line 6), whereby the contents of a data can be passed from one event to another event, each of said events having state information in a separate state information buffer (620) where the state information comprises a data buffer pointer pointing to a data buffer, and a context pointer pointing to a context buffer (page 22 line 28 – page 23 line 14).

Grounds of rejection to be reviewed on appeal

1. Whether claims 1, 3, 5 and 6 are unpatentable under 35 U.S.C. § 103(a) over Chong e al. (6,724,767) in view of Muller et al. (6,021,132).

2. Whether claim 10 is unpatentable under 35 U.S.C. § 103(a) over Chong e al. (6,724,767) in view of Muller et al. (6,021,132).

3. Whether claims 11, 13 and 15 are unpatentable under 35 U.S.C. § 103(a) over Chong e al. (6,724,767) in view of Muller et al. (6,021,132).

4. Whether claims 16 and 20 are unpatentable under 35 U.S.C. § 103(a) over Chong e al. (6,724,767) in view of Muller et al. (6,021,132).

ARGUMENT

OUTLINE

I. Summary of the brief on appeal.

II. Summary of the requirements for *prima facie* obviousness.

III. Claims 1, 3, 5 and 6 rejection.

IV. Claim 10 rejection.

V. Claims 11, 13 and 15 rejection.

VI. Claims 16 and 20 rejection.

I. Summary of the brief on appeal

A. The 35 U.S.C. § 103(a) rejection of claims 1, 3, 5 and 6 is improper because a *prima facie* case for obviousness has not been established, for the following reasons: (1) the cited art does not teach or suggest every element of the claims, (2) the examiner incorrectly characterizes the cited art.

B. The 35 U.S.C. § 103(a) rejection of claims 10 is improper because a *prima facie* case for obviousness has not been established, for the following reasons: (1) the cited art does not teach or suggest every element of the claims, (2) the examiner incorrectly characterizes the cited art.

C. The 35 U.S.C. § 103(a) rejection of claims 11, 13 and 15 is improper because a *prima facie* case for obviousness has not been established, for the following reasons: (1) the cited art does not teach or suggest every element of the claims, (2) the examiner incorrectly characterizes the cited art.

D. The 35 U.S.C. § 103(a) rejection of claims 16 and 20 is improper because a *prima facie* case for obviousness has not been established, for the following reasons: (1) the cited art does not teach or suggest every element of the claims, (2) the examiner incorrectly characterizes the cited art.

II. Summary of the requirements for *prima facie* obviousness.

MPEP 2143.03

The prior art reference (or references when combined) must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974).

If an independent claim is nonobvious under 35 U.S.C. 103, then any claim dependent therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

"To establish a prima facie case of obviousness, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings." MPEP 2142. "The teaching or suggestion to make the claimed combination... must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck*, 947 F.2ed 488, 20 USPQ2ed 1438 (Fed. Cir. 1991). "The level of skill in the art cannot be relied upon to provide the suggestion to combine references." *Al-Site corp. v. VSI Int'l Inc.*, 174 F.3d 1308, 50 USPQ2d 1161 (Fed. Cir. 1999). "The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggest the desirability of the combination" In re Mills, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990).

OTHER RELEVANT CASE LAW

"Factors including unexpected results, new features, solution of a different problem, novel properties, are all considerations in the determination of obviousness in terms of 35

U.S.C. § 103. When such factors are described in the specification they are weighed in determining, in the first instance, whether the prior art presents a prima facie case of obviousness." *In re Wright*, 6 U.S.P.Q.2d 1959, 1962 (Fed. Cir. 1988).

III. Claims 1, 3, 5 and 6 rejection.

Claim 1 has been finally rejected as being unpatentable under 35 U.S.C. § 103(a) over Chong e al. (6,724,767) in view of Muller et al. (6,021,132). Claim 1 is for an integrated circuit that comprises both a core processor and a co-processor. The co-processor circuitry comprises a plurality of state information buffers, a plurality of context buffers and a plurality of data buffers. The different buffers are on-chip hardware buffers. The data buffers 314 are relatively small and of a fixed size, such as 64 bytes, so if the packets are ATM cells, each data buffer holds only a single ATM cell and ATM cells do not cross data buffer boundaries (page 14 lines 11 – 19 and figures 3 and 6).

Chong does not have a plurality of state information buffers, context buffers, or data buffers formed as part of a co-processor. Chong forms a data structure comprising a two dimensional linked list. The buffers in chong are part of the data structure and are not part of the co-processor as required by claim 1.The data structure in chong is created dynamically for each VC and stored in the general internal memory of the chip (Column 5 lines 46 – 50) not in individual buffers.

Muller does not teach having a co-processor having state buffers, data buffers, and context buffers, where the state buffers store state information comprising a data buffer pointer pointing to a data buffer and a context pointer pointing to a context buffer.

The prior art reference (or references when combined) must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). Here, neither Chong or Muller teach "a co-processor having state buffers, data buffers, and context buffers, where the state buffers store state information comprising a data buffer pointer pointing to a data buffer and a context pointer pointing to a context buffer" therefore the cited prior art does not fulfilled the requirements for a *prima facie* case of obviousness. Therefore claims 1 is allowable as written.

Claims 3, 5 and 6 are dependent directly or indirectly on claim 1. If an independent claim is nonobvious under 35 U.S.C. 103, then any claim dependent therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988). Therefore claims 3, 5 and 6 are allowable as written.

IV. Claim 10 rejection.

Claim 10 has been finally rejected as being unpatentable under 35 U.S.C. § 103(a) over Chong e al. (6,724,767) in view of Muller et al. (6,021,132). Claim 10 is also for an integrated circuit comprising a core processor and a co-processor. The co-processor in claim 10 also has a plurality of state information buffers, a plurality of context buffers and a plurality of data buffers. As discussed above for claim 1, Chong does not teach a co-processor having a plurality of state information buffers, a plurality of context buffers and a plurality of data buffers formed as part of the co-processor hardware. Therefore claim 10 is also allowable as written.

IV. Claims 11, 13 and 15 rejection.

Claim 11 has been finally rejected as being unpatentable under 35 U.S.C. § 103(a) over Chong e al. (6,724,767) in view of Muller et al. (6,021,132). Claim 11 is a method of using an integrated circuit comprising a core processor and a co-processor. The co-processor in claim 11 also has a plurality of state information buffers, a plurality of context buffers and a plurality of data buffers. As discussed above for claim 1, Chong does not teach a co-processor having a plurality of state information buffers, a plurality of context buffers and a plurality of data buffers formed as part of the co-processor hardware. Therefore claim 11 is also allowable as written.

Claims 13 and 15 are dependent directly or indirectly on claim 11. If an independent claim is nonobvious under 35 U.S.C. 103, then any claim dependent therefrom is nonobvious.

In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988). Therefore claims 13 and 15 are allowable as written.

V. Claims 16 and 20 rejection.

Claim 16 has been finally rejected as being unpatentable under 35 U.S.C. § 103(a) over Chong e al. (6,724,767) in view of Muller et al. (6,021,132). Claim 16 is for an integrated circuit comprising a core processor and a co-processor. The co-processor in claim 16 has separate state information buffers, context buffers and data buffers. As discussed above for claim 1, Chong does not teach a co-processor having separate state information buffers, context buffers and data buffers formed as part of the co-processor hardware. Therefore claim 16 is also allowable as written.

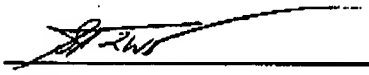
Claim 20 is dependent directly on claim 16. If an independent claim is nonobvious under 35 U.S.C. 103, then any claim dependent therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988). Therefore claim 20 is allowable as written.

Conclusion

In view of the above, applicant respectfully request that the examiner's rejection of claims 1, 3, 5, 6, 10, 11, 13, 15, 16, and 20 be reversed.

Respectfully submitted,

Date: 9/28/05



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APPENDIX I
CLAIMS CURRENTLY PENDING WITH THE PENDING AMENDMENT

1. An integrated circuit for processing events related to communication packets, said integrated circuit comprising:

a core processor configured to execute software to process a series of communication packets, the processing of each packet being an event and having associated data and context information; and

a co-processor comprising a plurality of state information buffers for storing state information, a plurality of context buffers for storing context information associated with a plurality of events and a plurality of data buffers for storing data associated with the plurality of events where the state information comprises a data buffer pointer pointing to one of the plurality of data buffers and a context buffer pointer pointing to one of the plurality of context buffers;

the state information is associated with events wherein each of said state information buffers ~~having~~ has an in-use counter indicating the number of events associated with the contents of said buffer.

2. (Canceled)

3. The integrated circuit of claim 1 wherein said co-processor comprises an in-use counter associated with each of said context buffers.

4. (Canceled)

5. (Currently amended) The integrated circuit of claim 1 wherein said co-processor comprises

an in-use counter associated with each of said data buffers.

6. (Currently amended) The integrated circuit of claim 1 wherein said plurality of data buffers each having an in-use counter whereby data can be transferred from one event to another event by changing information in a data buffer.

7. (Canceled)

8. (Canceled)

9. (Canceled)

10. An integrated circuit for processing events related to communication packets, said integrated circuit comprising:

a core processor configured to execute software to process a series of communication packets, the processing of each packet being an event and having associated data and context information; and

a co-processor comprising a plurality of state information buffers for storing state information associated with events wherein each of said state information buffers having an in-use counter indicating the number of events associated with the contents of said buffer, wherein said co-processor comprises a plurality of data only information buffers, a plurality of context information buffers, an in-use counter for each of said data only buffers and an in-use counter for each of said context buffers where data can be passed from one event to another event by changing the data in one of said state information buffers and where the state information comprises a data only buffer pointer pointing to one of the plurality of data only information buffers and a context information buffer pointer pointing to one of the pluralities of context information buffers.

11. A method of processing events related to communication packets in an integrated circuit which includes a core processor and a co-processor having a state information buffer for

storing state information, a context buffer for storing context information and a data buffer for storing data where the state information comprises a data buffer pointer and a context pointer where the data buffer pointer points to the data buffer and the context pointer points to the context buffer, the state information for an event is stored separate from the data associated with said event, said state information buffer having an associated in use counter, the method comprising:

incrementing the in-use counter associated with said state information buffer when an event is associated with said state information buffer; and

decrementing the in-use counter of said state information buffer when said event associated with said buffer is finished.

12. (Canceled)

13. (Currently amended) The method of claim 11 wherein said integrated circuit comprises an in-use counter for said context information buffer and the method further comprises:

incrementing the in-use counter associated with said context buffer when an event is associated with said context buffer; and

decrementing the in-use counter of said context buffer when said events associated with said context buffer is finished.

14. (Canceled)

15. The method of claim 11 wherein said integrated circuit comprises an in-use counter associated with said data buffer and the method further comprises:

incrementing the in-use counter associated with said data buffer when an event is associated with said data buffer; and

decrementing the in-use counter of said data buffer when said event associated with said data buffer is finished.

16. An integrated circuit for processing events associated with communication packets which

includes a core processor and a co-processor, the improvement which comprises, separate buffers for data, context, and state information and in-use counters for all of said buffers, whereby the contents of a data can be passed from one event to another event, each of said events having state information in a separate state information buffer where the state information comprises a data buffer pointer pointing to a data buffer, and a context pointer pointing to a context buffer.

17. (Canceled)

18. (Canceled)

19. (Canceled)

20. The integrated circuit of claim 16 which includes a plurality of data buffers, a plurality of state information buffers and a plurality of context information buffers, each of said plurality of data buffers and each of said plurality of state information buffers and each of said plurality of context buffers having an in-use counter which is incremented when an event is associated with one of the plurality of data buffers or with one of the plurality of state information buffers or with one of said plurality of context buffers and decremented when an event is finished utilizing one of the plurality of data buffers or with one of the plurality of state information buffers or with one of said plurality of context buffer.

21. (Canceled)

APPENDIX II

EVIDENCE SUBMITTED

None submitted.

APPENDIX III
RELATED PROCEEDINGS

No related proceedings.